

Notice of References Cited	Application/Control No. 10/696,203	Applicant(s)/Patent Under Reexamination HANSON ET AL.	
	Examiner Sun J. Lin	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,128,737	07-1992	van der Have	257/503
*	B	US-5,475,695	12-1995	Caywood et al.	714/738
*	C	US-6,701,477 B1	03-2004	Segal	714/732
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bichebois et al., "Analysis of Defect to Yield Correlation of Memories: Method, Algorithms and Limits", Oct. 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Proceedings pp. 44 - 52.
	V	Cheema et al., "Wafer Back Side Inspection Applications for Yield Protection and Enhancement", May 2002, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, Paper Digest pp. 64 - 71.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.